Alex K. Jones

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Professional Interests

Compilation techniques and novel architectures for SoCs, ASICs, and FPGAs, including, in particular, memory systems and interconnects for chip-multiprocessors and coarse-grain reconfigurable fabrics. Other interests include reliable computing, sustainable computing, wireless sensor networks/RFID, emerging memory technologies, and experimental reproducibility for computer science and engineering.

Education

Ph.D. September 2002, Northwestern University, Department of Electrical and Computer Engineering, Evanston, Illinois. Dissertation title: "PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations." Advisor: Prithviraj Banerjee.

M.Sc. September 2000, Northwestern University, Department of Electrical and Computer Engineering, Evanston, Illinois. Specialization: Computer-aided design and Parallel FPGA design.

B.Sc. May 1998, The College of William and Mary, *cum laude*, Major: Physics, Secondary Major: Music Performance. Thesis: Acoustic Music Synthesis, *high honors*.

Professional Positions Held

Professor, September 2017 - *current*: Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania

Professor, September 2017 - *current*: Department of Computer Science, University of Pittsburgh, Pittsburgh, Pennsylvania - *Secondary Appointment.*

Associate Director January 2018 - *current*: NSF Center for Space, High Performance, and Resilient Computing (SHREC), Pittsburgh, PA.

Director June 2013 - December 2017: Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania.

Associate Professor, September 2009 - August 2017: Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania

Associate Professor, September 2009 - August 2017: Department of Computer Science, University of Pittsburgh, Pittsburgh, Pennsylvania - *Secondary Appointment.*

Interim Director September 2011 - May 2013: Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania.

Visiting Researcher September 2010 - December 2010: Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, Virginia.

Assistant Professor, September 2003 - September 2009: Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania.

Assistant Professor, September 2005 - August 2009: Department of Computer Science, University of Pittsburgh, Pittsburgh, Pennsylvania - *Secondary Appointment.*

Visiting Researcher, 8/2003-9/2003: Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania.

Instructor, 9/2002-6/2003: Electrical and Computer Engineering, Northwestern University, Evanston, Illinois. Responsible for teaching core undergraduate and graduate courses in computer engineering, specifically, digital design, parallel computing, computer architecture, and computer-aided design.

Research Associate, 9/2002-7/2003: Center for Parallel and Distributed Computing (CPDC), Northwestern University, Evanston, Illinois. Post doctoral research responsibilities including research management and advising of M.Sc. and Ph.D. students, writing and reviewing papers, grant writing and review, and conducting original research.

Honors and Awards

Carnegie Science Award: Information Technology Category, 2017

MCSI Sustainability Faculty Fellowship: University of Pittsburgh, 2017

Top 25 paper of 20 years of FCCM, recognized April, 2013, paper originally published in 2000. Top 5% all time for this conference.

Best Paper Award, GLSVLSI, 2013.

Best Paper Nomination, DAC, 2013, ASPDAC 2014.

Dominion VITA Award, November 2012.

ACM SIGDA Service Award, June 2012.

Promoted to Senior member of the ACM, February, 2011.

ACM SIGDA Distinguished Service Award, June, 2010.

ACM SIGDA Service Award, July 2009.

Promoted to Senior member of the IEEE, July, 2008.

Pitt Innovator Award, 2007.

Featured Paper, Journal of Low Power Electronics, No. 1, Vol. 3, December 2005.

Walter P. Murphy Doctoral Fellowship, Northwestern University. Awarded twice in 1998 and again in 2000.

Graduated *cum laude*, The College of William and Mary, 1998.

Received *high honors* for senior research in Acoustic Music Synthesis as part of my B.Sc. in Physics from the College of William and Mary.

Publications

Refereed Journal Publications

1. S. Longofono, D. Kline, R. Melhem, A. K. Jones. *A CASTLE with TOWERs for Reliable, Secure PCM*, HPCA 2019 – *submitted*.
2. J. Zhang, D. Kline, L. Fang, R. Melhem, and A. K. Jones. *RETROFIT: Fault-aware Wear Leveling* IEEE Computer Architecture Letters, May 2018, DOI: 10.1109/LCA.2018.2840137.
3. D. Kline, R. Melhem, A. K. Jones. *Counter Advance for Reliable Encryption in Phase Change Memory* IEEE Computer Architecture Letters, 2018, DOI: 10.1109/LCA.2018.2861012.
4. J. Zhang, D. Kline, L. Fang, R. Melhem, and A. K. Jones. *Yielding Optimized Dependability Assurance through Bit Inversion*, Integration–The VLSI Journal, August 2018 DOI: 10.1016/j.vlsi.2018.09.002.
5. J. Zhang, D. Kline, L. Fang, R. Melhem, A. K. Jones, *Data Block Partitioning Methods to Mitigate Stuck-at Faults in Limited Endurance Memories*, IEEE Transactions on Very Large Scale Integration (TVLSI), June 2018, DOI: 10.1109/TVLSI.2018.2858186
6. D. Kline, H. Xu, R. Melhem, A. K. Jones, *Racetrack Queues for Extremely Low-Energy FIFOs*, IEEE Transactions on Very Large Scale Integration (TVLSI), April 2018, DOI: 10.1109/TVLSI.2018
7. D. Kline, N. Parshook, X. Ge, E. Brunvand, R. Melhem, P. Chrysanthis, A. K. Jones, *GreenChip: A Tool for Evaluating Holistic Sustainability of Modern Computing Systems*, Elsevier Journal of Sustainable Computing, Vol. 22(2019), June 2019, DOI=10.1016/j.suscom.2017.10.001 (https://doi.org/10.1016/j.suscom.2017.10.001).
8. S. M. Seyedzadeh, A. K. Jones, R. Melhem, *Counter-Based Tree Structure for Row Hammering Mitigation in DRAM*, IEEE Computer Architecture Letters, Volume: 16, Issue: 1, Jan.-June 1 2017, DOI=10.1109/LCA.2016.2614497.
9. H. Xu, Y. Alkabani, R. Melhem, and A. K. Jones, *FusedCache: A Naturally Inclusive, Racetrack Memory, Dual-Level Private Cache*, IEEE Transactions on Multi-Scale Computing Systems, Volume: 2, Issue: 2, April-June 1 2016, DOI=10.1109/TMSCS.2016.2536020
10. M. Moeng, A. K. Jones, R. Melhem, *Weighted-Tuple: Fast and Accurate Synchronization for Parallel Architecture Simulators*, IEEE Transactions on Parallel and Distributed Computing and Systems, 2015, DOI=10.1109/TPDS.2015.2494589.
11. M. Seyedzadeh, R. Maddah, A. K. Jones, and R. Melhem, *Improving Bit Flip Reduction for Biased and Random Data*, IEEE Transactions on Computers, 2016, DOI=10.1109/TC.2016.2525982
12. R. Khanna, V. Vahdat, K. Gassei, C. Ishwad, J. Erickson, A. K. Jones, W. E. Stanchina, and A. Vats, *Low-cost, portable, isothermal nucleic acid detection with handheld, mobile device connectivity*, PLOS ONE, *in revision*.
13. B. R. Childers, A. K. Jones, and D. Moss, *A Roadmap and Plan of Action for for Community-Supported Empirical Evaluation in Computer Architecture*, ACM SIGOPS Operating Systems Review, Vol. 49, No. 1, January 2015, pp. 108-117, DOI=10.1145/2723872.2723886
14. M. Moeng, H. Xu, R. Melhem, A. K. Jones, *ContextPreRF: Enhancing The Performance and Energy of GPUs with Non-Uniform Register Access (NURA)*, IEEE Transactions of Very Large Scale Integration (TVLSI) Briefs, Vol. 24, No. 1, January 2016, pp. 343-347, DOI=10.1109/TVLSI.2015.2397876.

15. E. Sejdic, A. Millecamps, J. Teoli, M. A. Rothfus, N. G. Franconi, A. K. Jones, J. S. Brach, and M. H. Mickle, *Assessing interactions among multiple physiological systems during walking outside a laboratory: An Android based gait monitor*, Computer Methods and Programs in Biomedicine, Volume 122, Issue 3, December 2015, Pages 450-461, ISSN 0169-2607, DOI=10.1016/j.cmpb.2015.08.012.

16. H. Xu, W. O. Collinge, L. A. Schaefer, A. E. Landis, M. M. Bilec, A. K. Jones, *Towards a Commodity Solution for the Internet of Things*, Elsevier Journal of Computers and Electrical Engineering, Volume 52, May 2016, Pages 138156, DOI=10.1016/j.compeleceng.2016.03.009.

17. Y. Li, R. Melhem, A. K. Jones, *A Practical Data Classification Framework for Scalable and High Performance Chip-Multiprocessors*, IEEE Transactions on Computers, Vol. 63, No. 12, December 2014 pp. 2905–2918, DOI=10.1109/TC.2013.161,

18. Y. Li, Y. Zhang, H. Li, Y. Chen, A. K. Jones, *C1C: A Configurable, Compiler-guided STT-RAM L1 Cache*, ACM Transactions on Architecture and Code Optimization (TACO), Vo. 10, No. 4, December 2013, Article No. 52, pp. 52:1-52:22, DOI=10.1145/2541228.2555308 http://dx.doi.org/10.1145/2541228.2555308. (Citations: 14)

19. A. Abousamra, A. K. Jones, and R. Melhem, *Ordering Circuit Establishment in Multiplane NoCs*, ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 18, No. 4, October 2013, Article No. 49, pp. 49:1-49:33, DOI=10.1145/2500752 http://doi.acm.org/10.1145/2500752

20. Y. Li, Y. Zhang, Z. Sun, H. Li, Y. Chen, and A. K. Jones, *Read Performance: The Newest Barrier in Scaled STT-RAM*, IEEE Transactions on Very Large Scale Integration Briefs, Vol. 23, No. 6, pp. 1170-1174, June 2015. DOI=10.1109/TVLSI.2014.2326797. (Citations: 24)

21. Y. Anil, J. Stander, A. K. Jones, G. Mehta, *A Study of Energy-Area Tradeoffs of Various Architectural Styles for Routing Inputs in a Domain Specific Reconfigurable Fabric*, International Journal of VLSI Design Communication Systems. Vol 4, 2013, pp. 73-91. DOI: 10.5121/vlsic.2013.4107.

22. G. Mehta, A. K. Jones, *Implementation and validation of architectural space exploration techniques for domain-specific reconfigurable computing*, Design Automation of Embedded Systems, 2013 vol. 17, pp. 2751 DOI: 10.1007/s10617-013-9118-1

23. C. Saunders, A. E. Landis, L. P. Mecca, A. K. Jones, L. A. Schaefer, and M. M. Bilec, *Analyzing the Practice of Life Cycle Assessment: Focus on the Building Sector*, Journal of Industrial Ecology, available online, May, 2013, DOI: 10.1111/jiec.12028.

24. Y. Li, R. Melhem, and A. K. Jones, *PS-TLB: Leveraging Page Classification Information for Fast, Scalable and Efficient Translation for Future CMPs*, ACM Transactions on Architecture and Code Optimization (TACO), Vol. 9, Issue 4, January 2013, DOI 10.1145/2400682.2400687.

25. Y. Li, Y. Zhang, Y. Chen, and A. K. Jones, *Combating Write Penalties Using Software Dispatch for On-Chip MRAM Integration*, IEEE Embedded Systems Letters, Vol. 4, No. 4, Dec. 2012.

26. C. L. Thiel, N. Campion, A. E. Landis, A. K. Jones, L. A. Schaefer, M. Bilec, *A Materials Life Cycle Assessment of a Net-Zero Energy Building*, Energies, Vol. 6, No. 2, pp 1125-1141, Feb. 2013, DOI: 10.3390/en6021125. (Citations: 33)

27. W. O. Collinge, A. E. Landis, A. K. Jones, L. A. Schaefer, M. M. Bilec. *Indoor environmental quality in a dynamic life cycle assessment framework for whole buildings: Focus on human health chemical impacts.* Buildings and the Environment, 62, Apr. 2013, pp. 182-190. DOI=10.1016/j.buildenv.2013.01.015 http://dx.doi.org/10.1016/j.buildenv.2013.01.015. (Citations: 23)

28. W. O. Collinge, A. E. Landis, A. K. Jones, L. A. Schaefer, M. M. Bilec. *A Dynamic Life Cycle Assessment: Framework and Application to an Institutional Building.* International Journal of Life Cycle Assessment, Vol. 18 No. 3, Mar. 2013, pp. 538-552. DOI=10.1007/s11367-012-0528-2 http://dx.doi.org/10.1007/s11367-012-0528-2 (Citations: 52)

29. Y. Li, R. Melhem, A. K. Jones, *Leveraging Sharing in Second Level Translation-Lookaside Buffers for Chip Multiprocessors* IEEE Computer Architecture Letters, Vol. 11, No. 1, July-Dec. 2012, DOI:10.1109/L-CA.2011.35.
30. Y. Li, A. Abousamra, R. Melhem, A. K. Jones, *Compiler-assisted Data Distribution and Network Configuration for Chip Multiprocessors* IEEE Transactions of Parallel and Distributed Computing, Vol. 23, No. 11, November 2012, pp. 2058-2066. DOI: 10.1109/TPDS.2011.279
31. A. Abousamra, A. K. Jones, R. Melhem, *Co-Design of NoC and Cache Organization for Reducing Access Latency in Chip Multiprocessors,* IEEE Transactions of Parallel and Distributed Computing, Volume 23, Number 6, June 2012, pp. 1038-1046. DOI: 10.1109/TPDS.2011.238. (Citations: 15)
32. A. K. Jones, D. J. Kerbyson, R. Rajamony, and C. Weems, *Guest Editor's Note: Large-Scale Parallel Processing,* Parallel Processing Letters, Vol. 19, No. 4, 2009, pp. 487-490.
33. Y. Zhang and A. K. Jones, *Non-Uniform "Fat-Meshes" For Chip Multiprocessors,* Parallel Processing Letters, Vol. 19, No. 4, 2009, pp. 595-617.
34. A. K. Jones, D. J. Kerbyson, R. Rajamony, and C. Weems, *Guest Editor's Note: Large-Scale Parallel Processing,* Parallel Processing Letters, Vol. 18, No. 4, 2008, pp. 449-451.
35. A. K. Jones, S. Shao, Y. Zhang, and R. Melhem, *Symbolic Expression Analysis for Compiled Communication,* Parallel Processing Letters, Vol. 18, No. 4, 2008, pp. 567-587.
36. R. Hoare, Z. Ding, and A. K. Jones, *A Two-stage Hardware Scheduler for Large Cardinality Crossbar Switches*, Journal of Parallel and Distributed Computing (JPDC), Vol. 68, No. 11, 2008, pp. 1437-1451.
37. G. Mehta, J. Stander, M. Baz, B. Hunsaker, and A. K. Jones *Interconnect Customization for a Hardware Fabric*, ACM Transactions on Design Automation for Electronic Systems (TODAES) - Vol. 14, No. 1, 2009, pp. 1-32, Article 11, DOI 10.1145/1455229.11455240. (Citations: 14)
38. S. Dontharaju, S. Tung, J. T. Cain, L. Mats, M. H. Mickle, and A. K. Jones, *A Design Automation and Power Estimation Flow for RFID Systems*, ACM Transactions on Design Automation for Electronic Systems (TODAES) - Vol. 14, No. 1, 2009, pp. 1-31, Article 7, DOI 10.1145/1455229.1455236. (Citations: 11)
39. S. Shao, A. K. Jones, and R. Melhem, *Compiler Techniques for Efficient Communications in Circuit Switched Networks for Multiprocessor Systems*, IEEE Transactions for Parallel and Distributed Systems (TPDS), Vol. 20, No. 3, pp. 331-345. (Citations: 13)
40. A. K. Jones, R. A. Walker, *Introduction to the Special Issue on Demonstrable Software Systems and Hardware Platforms II*, ACM Transactions on Design Automation for Electronics Systems (TODAES), Vol. 13, No. 3, Article 38, July, 2008, DOI 10.1145/1367045.1367047.
41. A. K. Jones, S. Dontharaju, S. Tung, L. Mats, P. Hawrylak, R. R. Hoare, J. T. Cain, and M. H. Mickle, *Radio Frequency Identification Prototyping*, ACM Transactions on Design Automation for Electronic Systems (TODAES), Vol. 13, No. 2, April, 2008, pp. 1-21, Article 29, DOI 10.1145/1344418.1344425. (Citations: 11)
42. M. H. Mickle, J. T. Cain, A. K. Jones, *Intellectual Property and Ubiquitous RFID*, Recent Patents on Electrical Engineering, Vol. 1, No. 1, January 2008, pp. 59-67.
43. A. K. Jones, R. Hoare, S. Dontharaju, S. Tung, R. Sprang, J. Fazekas, J. T. Cain, M. H. Mickle, *An Automated, FPGA-based Reconfigurable, Low-Power RFID Tag*, Journal of Microprocessors and Microsystems, Vol. 31, No. 2, March 2007, pp. 116-134. (Citations: 43)
44. S. Dontharaju, S. Tung, A. K. Jones, L. Mats, J. Panuski, J. T. Cain, and M. H. Mickle, *The Unwinding of a Protocol*, IEEE Applications and Practice - April, 2007, Vol. 1, No. 1, pp. 4-9.
45. A. K. Jones, R. Hoare, D. Kusic, J. Fazekas, G. Mehta, and J. Foster, *A VLIW Processor with Hardware Functions: Increasing Performance While Reducing Power*, IEEE Transactions on Circuits and Systems II, Vol. 53, No. 11, November 2006, pp. 1250-1254. (Citations: 14)

46. A. K. Jones, S. Dontharaju, S. Tung, P. Hawrylak, L. Mats, R. Hoare, J. T. Cain, M. H. Mickle, *Passive Active Radio Frequency Identification Tags (PART)*, International Journal of Radio Frequency Identification Technology and Applications (IJRFITA) - Vol. 1, No. 1, 2006, pp. 52-73. (Citations: 21)
47. J. M. Lucas, R. Hoare, I. S. Kourtev, A. K. Jones, *Technology Mapping for Field Programmable Gate Arrays using Content-Addressable Memory (CAM)*, Journal of Microprocessors and Microsystems - Vol. 30, No. 7, November, 2006, pp. 445-456.
48. A. K. Jones, R. Hoare, D. Kusic, G. Mehta, J. Fazekas, and J. Foster, *Reducing Power while Increasing Performance with SuperCISC*, ACM Transactions on Embedded Computing Systems (TECS) - Vol. 5, No.3, August 2006, pp. 658-686. (Citations: 30)
49. J. Schuster, K. Gupta, R. Hoare, and A. K. Jones, *Speech Silicon: An FPGA Architecture for Real-time, Hidden Markov Model Based Speech Recognition*, EURASIP Journal on Embedded Systems (JES), Vol. 2006, Article ID 48085, 2006, Pages 1-19. (Citations: 26)
50. G. Mehta, R. R. Hoare, J. Stander, J. Lucas, B. Hunsaker, and A. K. Jones, *A Low-Energy Reconfigurable Fabric for the SuperCISC Architecture*, Journal of Low Power Electronics (JOLPE) - Vol. 2, No. 2, August 2006, pp. 148-164. (Citations: 17)
51. P. J. Hawrylak, L. Mats, J. T. Cain, A. K. Jones, S. Tung, M. H. Mickle, *Ultra Low-power Computing Systems for Wireless Devices*, International Review on Computers and Software (IRECOS), Vol. 1, No. 1, July 2006, pp. 1-10.
52. R. Hoare, A. K. Jones, D. Kusic, J. Fazekas, J. Foster, S. Tung, M. McCloud, *Rapid VLIW Processor Customization For Signal Processing Applications Using Combinational Hardware Functions*, EURASIP Journal on Applied Signal Processing (JASP), Vol. 2006, Article ID 46473, 2006, pp. 1-23. (Citations: 38)
53. A. K. Jones, J. Zhang, A. Amer, *Entropy Based Evaluation of Communication Predictability in Parallel Applications*, IEICE Transactions on Information & Systems, Vol. E89-D, No. 2, February 2006, pp. 469-478.
54. X. Tang, T. Jiang, A. Jones, and P. Banerjee, *Behavioral Synthesis with power Estimation and Optimization for Unscheduled Data-Dominated Circuits*, Journal of Low Power Electronics, Vol. 1, No.3, December 2005, pp. 259-272. (Citations: 12)
55. R. Hoare, Z. Ding, S. Tung, Rami Melhem, and A. K. Jones, *A Framework for the Design, Synthesis and Cycle-Accurate Simulation of Multiprocessor Networks*, Journal of Parallel and Distributed Computing, Vol. 65, No. 10, October 2005, pp. 1237-1252.

Books

1. C. Ihrig and A. K. Jones, *Improving Performance and Reducing Power with Hardware Acceleration: Static Timing Analysis Based transformation of Combinational Logic in an High Level ASIC Synthesis Flow*, VDM Publishing.

Chapters in Edited Books

1. M. Bedewy, M. Abdelhakim, and A. K. Jones, *Cybermanufacturing - recent technologies, promising paradigms and future challenges*, Chapter 6 in "Advances in manufacturing and processing of materials and structures," Y. Bar-Cohen, editor, CRC Press/Taylor & Francis Group, LLC., *to appear*
2. C. Ihrig, M. Baz, J. Stander, R. R. Hoare, B. A. Norman, O. Prokopyev, B. Hunsaker, and A. K. Jones, *Greedy Algorithms for Mapping onto a Coarse-grained Reconfigurable Fabric*, Chapter 11 in "Advances in Greedy Algorithms", V. Kordic, editor, I-Tech Education and Publishing, Vienna, Austria, October 2008, pp. 193-222.

3. S. Dontharaju, S. Tung, R. R. Hoare, M. H. Mickle, J. T. Cain, A. K. Jones *Design Automation for RFID Tags and Systems*, Chapter 3 in "RFID Handbook: Applications, Technology, Security, and Privacy," S. Ahson and M. Ilyas, editors, Taylor and Francis, March 2008, pp. 35-64.
4. S. Tung, S. Dontharaju, L. Mats, P. J. Hawrylak, M. H. Mickle, J. T. Cain, A. K. Jones, *Layers of Security for Active RFID Tags*, Chapter 33 in "RFID Handbook: Applications, Technology, Security, and Privacy." S. Ahson and M. Ilyas, editors, Taylor and Francis, March 2008, pp. 603-630.
5. A. K. Jones, S. Tung, S. Dontharaju, G. J. Dhanabalan, P. J. Hawrylak, L. Mats, M. H. Mickle, and J. T. Cain, *Minimum Energy/Power Considerations*, Chapter 11 in "RFID Handbook: Applications, Technology, Security, and Privacy." S. Ahson and M. Ilyas, editors, Taylor and Francis, March 2008, pp. 199-230.
6. A. Jones, D. Bagchi, S. Pal, P. Banerjee, A. Choudhary. *A Compiler with Power and Performance Optimizations*, appears in "Power Aware Computing," R. Graybill, R. Melhem, editors, Kluwer Academic Publishers, 2002. (Citations: 17)

Refereed Conference Proceedings (full papers)

1. D. Kline, R. Melhem, A. K. Jones. *FLOWER and FaME: A Low Overhead Bit-level Fault-map and Fault-tolerance Approach for Deeply Scaled Memories*, IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2020.
2. S. Longofono, D. Kline, R. Melhem, A. K. Jones, *Toward Secure, Reliable, and Energy Efficient Phase-change Main Memory with MACE*, IGSC, 2019.
3. D. Kline, S. Longofono, S. Ollivier, E. Higgins, R. Melhem, and A. K. Jones, *PREMSim: A Resilience Framework for Modeling Traditional and Emerging Memory Reliability*, MASCOTS, 2019.
4. D. Kline, S. Longofono, R. Melhem, and A. K. Jones, *Predicting Single Event Effects in DRAM*, DFT, 2019.
5. S. Ollivier, D. Kline, R. Kawsher, R. Melhem, S. Banja, A. K. Jones. *Leveraging Transverse Reads to Correct Alignment Faults in Domain Wall Memories*, DSN 2019.
6. M. Seyedzadeh, A. K. Jones, R. Melhem. *Improving Sustainability Through Disturbance Crosstalk Mitigation in Deeply Scaled Phase-change Memory*, IEEE International Green and Sustainable Computing Conference (IGSC), October 2018 – *Best Paper Nominee*.
7. E. Brunvand, D. Kline, A. K. Jones. *Dark Silicon Considered Harmful*, IEEE International Green and Sustainable Computing Conference (IGSC), October 2018 – *Best Paper Award*.
8. M. Seyedzadeh, A. K. Jones, and R. Melhem, *Mitigating Wordline Crosstalk using Adaptive Trees of Counters*, ISCA, 2018.
9. M. Seyedzadeh, A. K. Jones, and R. Melhem, *Enabling Fine-Grain Restricted Coset Coding Through Word-Level Compression for PCM*, HPCA, 2018.
10. J. Zhang, D. Kline, R. Melhem, and A. K. Jones, *Yoda: Judge me by my size, do you? Dramatically Improving Error Mitigation Through Small Increases in Encoding Bits*, IEEE International Conference on Computer Design (ICCD), 2017.
11. J. Zhang, D. Kline, R. Melhem, and A. K. Jones, *Dynamic Partitioning to Mitigate Stuck-at Faults in Emerging Memories*, IEEE/ACM International Conference of Computer-Aided Design (ICCAD), 2017.
12. D. Kline, N. Parshook, A. Johnson, J. E. Stine, W. Stanchina, E. Brunvand, A. K. Jones, *Sustainable IC Design and Fabrication*, IEEE International Green and Sustainable Computing Conference (IGSC), October 2017.

13. D. Kline, R. Melhem, A. K. Jones, *Holistic Energy Efficient Crosstalk Mitigation in DRAM*, IEEE International Green and Sustainable Computing Conference (IGSC), October 2017.
14. D. Kline, R. Melhem, A. K. Jones, *Sustainable Fault Management and Error Correction for Next-Generation Main Memories*, IEEE International Green and Sustainable Computing Conference (IGSC), October 2017.
15. S. M. Seyedzadeh, D. Kline, A. K. Jones, R. Melhem, *Mitigating Bitline Crosstalk Noise in DRAM Memories*, MEMSYS, 2017.
16. D. Kline, N. Parshook, E. Brunvand, R. Melhem, P. K. Chrysanthis, A. K. Jones, *Holistically Evaluating the Environmental Impacts in Modern Computing Systems*, IEEE International Green and Sustainable Computing and Systems (IGSC), 2016.
17. I. Bayram, E. Eken, D. Kline, N. Parshook, Y. Chen, and A. K. Jones, *Modeling STT-RAM Fabrication Cost and Impacts in NVSim*, IEEE International Green and Sustainable Computing and Systems (IGSC), 2016.
18. Y. Alkabani, Z. Koopmans, H. Xu, A. K. Jones, and R. Melhem, *Write Pulse Scaling for Energy Efficient STT-MRAM*, IEEE International Symposium on VLSI (ISVLSI), 2016.
19. S. M. Seyedzadeh, R. Maddah, A. K. Jones, R. Melhem, *Leveraging ECC to Mitigate Read Disturbance, False Reads and Write Faults in STT-RAM*, IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), 2016.
20. H. Xu, M. M. Bilec, W. O. Collinge, L. A. Schaefer, A. E. Landis, and A. K. Jones, *Improving Efficiency of Wireless Sensor Networks Through Lightweight In-Memory Compression*, IEEE International Green and Sustainable Computing Conference (IGSC), 2015. DOI: 10.1109/IGCC.201
21. H. Xu, M. M. Bilec, W. O. Collinge, L. A. Schaefer, A. E. Landis, and A. K. Jones, *Lynx: A Self-Organizing Wireless Sensor Network with Commodity Palmtop Computers*, ACM System Level Internet Prediction Workshop, 2015. DOI: 10.1109/SLIP.2015.7171712
22. D. Kline, H. Xu, F. Chen, R. Melhem, A. K. Jones, *Domain-wall memory Buffer for Low-Energy NoCs*, IEEE/ACM Design Automation Conference (DAC), 2015. DOI: 10.1145/2744769.2744826
23. M. Seyedzadeh, R. Maddah, A. K. Jones, R. Melhem, *PRES: A Pseudo-Random Encoding Scheme to Increase Bit Flip Reduction in Memory*, IEEE/ACM Design Automation Conference (DAC), 2015. DOI: 10.1145/2744769.2755440
24. Y. Li, H. Xu, R. Melhem, A. K. Jones, *Space Oblivious Compression: Power Reduction for Non-Volatile Main Memories*, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2015. DOI: 10.1145/2742060.2742107
25. D. Kline, K. Wang, R. Melhem, A. K. Jones, *MSCS: Multi-hop Segmented Circuit Switching*, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2015. DOI: 10.1145/2742060.2742087
26. M. Moeng, R. Melhen, A. K. Jones, *Reciprocal Abstraction for Computer Architecture Co-Simulation*, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2015. DOI: 10.1109/ISPASS.2015.7095812
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Technical Reports and Popular Journals

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Patents

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Invited Presentations

GLSVLSI *Green Computing: Challenges and Opportunities*, GLS Symposium on VLSI, May 2017 *Keynote.*

U. Utah *Green Computing: Challenges and Opportunities*, University of Utah, March 2017.

WVU *Shifting the Focus to Spintronic Domain Wall Memories*, West Virginia University, April 2016.

SAMSUNG *Constructing Scalable, Energy Efficient and Reliable Main Memory with STT-RAM*, Samsung MRAM Forum, Invited Talk, Nov. 2015.

ICCAD *Extreme Scale Design Automation*, Panel Keynote, ICCAD Conference, Nov. 2014.

SAMSUNG *Constructing Scalable, Energy Efficient and Reliable Main Memory with STT-RAM*, Colloquium Talk, Samsung, Nov. 2014.

NSF *Extreme Scale Design Automation: Report to the NSF*, April 29, 2014.

GLSVLSI *EDA for Extreme Scale Systems: Design Abstractions, Metrics, and Benchmarks*, May 23, 2014. *Keynote*

ICCAD *Considering Fabrication in Sustainable Computing*, Invited Talk, ICCAD, Nov. 2013.

ISVLSI *Cross-Layer Techniques for Optimizaing System Utilizing Memories with Asymmetric Access Characteristics*, Invited Talk, ISVLSI, Aug. 2012.

Virginia Tech *Low-energy Reconfigurable Computing*, Presentation, November 9th, 2007.

Westinghouse, Inc. *Hardware Devices and Electronic Design Automation*, Presentation, August, 6th 2004.

Northrup Grumman, Corp. *The Data Forest Supercomputer*, Presentation, April 21st, 2004.

Illinois Institute of Technology *PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations*, Presentation, March 5th, 2003.

University of Tennessee *PACT HDL: A Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations*, Presentation, March, 2003.

Grants

Current

LPS *Improving Energy Efficiency and Reliability of Emerging Memories*, PI, $120,000, 01/01/2018 - 12/31/2018.

NSF *I/UCRC: SHREC*, Co-PI with A. George (PI), J. Yang, and E. Sejdic, 09/01/2017 - 08/30/2022.

Completed

NSF *CI-ADDO-NEW: OCCAM: Open Curation for Computer Architecture Modeling*, Co-PI with B. Childers (PI), and D. Mossé, $200,000, 09/01/2013 - 08/31/2015.

NSF *CCF Core Programs: SHF:Medium:Compiler and Chip Multiprocessor Co-design for Scalable Efficient Data Access and Communication*, PI with R. Melhem and S. Cho, $800,000, 3/15/11 - 3/14/17.

NSF *EFRI-SEED: BUILD - Barriers, Understanding, Integration - Life Cycle Development*, Co-PI with M. Bilec (PI), A. Landis, L. Schaefer, and S. Lee (CMU), $2,052,981, 8/15/2010 - 7/31/2017.

SAMSUNG *Constructing Scalable, Energy Efficient and Reliable Main Memory with STT-MRAM*, Co-PI with R. Melhem (PI),$252,679, 02/15/2014 - 02/14/2017.

LPS *OCCAM: Open Curation for Computer Architecture Modeling*, Co-PI with B. Childers (PI), and D. Mossé, $100,000, 09/01/2014 - 08/31/2015.

CCC *CCC Visioning Proposal: Extreme-Scale Design Automation*, PI with P. Madden (SUNY Binghamton), I. Markov (Michigan), D. Marculescu (CMU), I. Bahar (Brown), and S. Katkoori (South Florida), $79,992, 6/1/2012 - 5/31/2014.

NSF *CRI: CI-P: An Innovative Dual-Path Computer Architecture Modeling Infrastructure for Highly Productive System Simulation and Emulation*, Co-PI with S. Cho (PI) and R. Melhem, $100,000, 2/1/11 - 1/31/13.

NSF *I/UCRC: Nexys: Next Generation Electronic System Design*, PI with S. Levitan, J. Yang, Y. Chen collaborative with CMU (lead, D. Marculescu PI) and Penn State (V. Narayanan PI), $11,500, 4/1/2012 - 3/31/2013.

BFTDA *Power & Energy: Interfaces Of Nuclear, Mining And Electric Power Engineering Initiative Project Summary*, Co-PI with B. Gleeson (PI), G. Reed (PI), Z. Mao.

The Technology Collaborative *Computer Engineering Laboratory Upgrade*, PI with S. Levitan, $75,000, 07/01/07 - 06/30/10.

National Science Foundation *NSF Foundations of Computing Processes and Artifacts: Enabling Circuit Switching with Compiler and Runtime Analysis for High Performance Systems*, PI with R. Melhem, $325,000, 05/01/2007 - 04/30/2010.

Synplicity, Inc. *FPGA and ASIC Computer Aided Design Tools Donation*, Fair Market Value $57,772,500, 07/01/2004 - 06/30/2009.

The Technology Collaborative *Hardware Fabrics: Embedded Solutions for High Performance and Micro Power.*, $298,070, 03/01/2007 - 02/28/2009.

Swanson Institute for Technical Excellence *An Ultra Low-power, Gen 2 Compatible Active RFID Tag*, $39,800, PI with M. H. Mickle, J. T. Cain, J. Rajgopal, and B. A. Norman, 08/01/2006 - 07/31/2007.

Swanson Institute for Technical Excellence *Optimizing Antenna/Reader Placement for Arbitrary Orientations of Passive RFID Tags*, $39,800, Co-PI with J. Rajgopal (PI), B. A. Norman, M. H. Mickle, and J. T. Cain, 08/01/2006 - 07/31/2007.

University of Pittsburgh *A Low-Energy Computing Fabric with Design Flow*, $37,106, 07/01/2006 - 06/31/2007.

The Technology Collaborative *Electronic Design Education Program Digital Sandbox Course Collaboration*, $27,330, PI, 08/01/2006-12/31/2006.

National Instruments *National Instruments Equipment Grant Proposal*, $50,000, Co-PI, with M. H. Mickle (PI), and J. T. Cain.

The Technology Collaborative *SECuRFID: Secure, Efficient, Customizable RFID Systems*, $30,000, PI with M. H. Mickle and J. T. Cain, 07/01/2006 - 12/31/2006.

Tego, Inc. *RF Front-End Integration and Testing with Atlas*, $59,000, Co-PI with M. H. Mickle (PI), and J. T. Cain, 8/1/2006 - 12/31/2006.

The Technology Collaborative *Enabling a Low-power, Secure RFID Tag*, PaCSCI Phase I Grant, $10,049, 10/1/2005 - 06/30/2006.

Xilinx, Inc. *XUP Software Donation for FPGA and Embedded Computing Development for Research and Teaching Labs, 200 seats*, Fair Market Value $3,735,000, 05/25/05.

ADCUS, Inc. *Development Tools and Microprocessor Development System*, Fair Market Value $400,000, Co-PI, with J. T. Cain, R. Hoare, and M. Mickle (PI).

IBM/DARPA *Productive, Easy to use, Reliable Computer Systems, High Productivity Computing Systems (HPCS) - Phase II*, $900,000, 09/01/03 - 08/31/06, Co-PI, with R. Melhem (PI), A. Amer, R. Hoare.

Pittsburgh Digital Greenhouse *Digital Sandbox Maintainance Grant*, $75,000, 07/01/04 - 06/30/05, Co-PI with T. Cain, I. Kourtev, S. Levitan, R. Hoelzeman.

ADCUS, Inc. *An RFID Tag Generation System for the ADCUS EISC 16 Bit Processor and Design Environment*, $175,947, 09/01/04 - 08/31/05, Co-PI, with M. Mickle (PI), T. Cain, and R. Hoare.

Swanson Center for Micro and Nano Systems *Efficient, Low-Power Computing for Micro and Nano Systems: Exploiting Different Forms of Parallelism*, $30,800, 08/01/04 - 07/31/05, PI, with R. Hoare.

Xilinx, Inc. *XUP Software Donation*, Fair Market Value $18,675, 10/01/04 - 09/30/04.

Courses Taught

University of Pittsburgh

ECE 2195 Sustainable Computing – Introduction to holistic sustainability for computing including life cycle methods, low power computing, and computing for sustainable applications.

ECE 2120 Hardware Design Methodologies – Introduction to hardware design methodologies through use of industry tools. Students use design automation tools to design, simulate, and synthesize designs for ASICs and FPGAs using hardware description languages (e.g. VHDL, Verilog, and/or SystemC). Techniques for design optimization, simulation, and synthesis of combinatorial functions, data paths, and finite state machines are covered in depth.

ECE 2130(3131) VLSI-CAD – Introduction to the fundamental concepts to building computer-aided design tools for VLSI. Topics include fundamental data structures including cubes and BDDs, algorithms for logic minimization, placement and routing of standard cells, verification, etc. Students complete homework assignments, and programming projects.

ECE 2140 System-on-a-Chip Design (SoC) – Students learn fundamental concepts of building an SoC. Topics include hardware and software partitioning, design and reuse of intellectual property blocks, design specification. All students work on different components of a term long SoC design targeted for actual hardware (typically an FPGA containing embedded hard core processor(s)). The students are tasked with making progress report presentations, communication between groups, creating interface specifications. Appropriate papers and homeworks are assigned.

ENGR 1905 Emerging Topics in Sustainability – Cross disciplinary course to introduce new and emerging topics in sustainability to a wide audience.

ECE/CoE 1896 Senior Design – Students are tasked with completing a semester long project within an interdisciplinary team as the Capstone of their curriculum. Lecture topics include proposal preparation, project management, budgeting, development of milestones and deliverables, project reporting, and preparation of a peer-reviewed technical document (e.g., IEEE Letters Paper). Discussion of the project extends beyond traditional technical matters into elements of ethics, sustainability, globalization, economic factors, and more.

ECE/CoE 1885 Undergraduate Seminar – Students are exposed to a mixture of technical and non-technical material. Technical topics include introductions to research areas ECE/CoE faculty, active projects in industry, and interdisciplinary topics and programs, principally through guest lectures. Non-technical topics include ethics, leadership, lifelong learning, and globalization.

ECE 1570 Special Topics – Pilot course of data structures and algorithms in C++.

ECE/CoE 0501 Digital Systems Laboratory (course director) – A sequence of laboratory assignments to reinforce material from EE/CoE 0132 through building of combination and sequential circuits eventually building a simple datapath with register file and ALU. Students learn to use a breadboard, Oscilloscope, Logic Analyzer, a schematic editor, and FPGA.

ECE/CoE 0132 Digital System Design – Introduction to the fundamentals of digital systems and design including logic gates, boolean algebra, karnaugh maps, transistor schematics, flip-flops, arithmetic units, and finite state machines.

Northwestern University

ECE 397 Introduction to ASIC and FPGA Design – Introduction to the process of designing application specific hardware implementations of algorithms for ASICs and FPGAs. Students work with commercial high-level synthesis tools and hardware description languages to realize these designs. Topics covered include register transfer level design, finite state machines, design reuse and intellectual property cores, and memory pipelining.

ECE 203 Introduction to Computer Engineering – Provides an introduction to computer engineering concepts, both hardware and software, with emphasis placed on digital logic concepts. Topics include binary number representations, Boolean algebra, simplification methods for combinational circuits, introduction to sequential circuits, introduction to assembly language programming, and networks. The concepts are applied to a hands-on laboratory assignments that includes hardware and software designs of a controller to navigate a robot through a given obstacle course.

ECE 303 Advanced Digital Design – Advanced topics in digital design from two-level to multi-level combinational logic, finite state machine design, minimization, and synthesis. Introduction of contemporary computer-aided design (CAD) tool theory and use for optimization. Introduction of hardware description languages for combinational and sequential circuits.

ECE 361 Computer Architecture – Teaches the design of a complete computer system. Design topics include instruction set architectures, datapaths, control, memory hierarchies such as main memory, caches and virtual memory, and I/O systems. Students work with commercial CAD tools to design a simple ALU and single cycle processor covering these topics.

ECE 358 Introduction to Parallel Computing – Provides an introduction to the field of parallel computing. Includes an overview of three basic parallel computing paradigms: shared memory, distributed memory message passing, and data parallel computing. These concepts are reinforced with hands-on experience with real parallel programming on actual parallel machines.

Student Supervision

Doctoral Dissertations Supervised

Haifeng Xu – Sensor network design and integration of new computer architectures and memory systems sustainable instrumentation of green buildings and renewable energy integration.

Michael Moeng – Simulation of Manycore Architectures on Multicore Hosts – *co-advised with Rami Melhem*

Yong Li – Compilers for Improving Performance of Reconfigurable Multi-core Systems – now at VMWare, Inc.

Ahmed Abousamra – Network-on-chip architectures for low-latency and low-power applications in chip-multiprocessors – now at Intel. – *Co-Advised with Rami Melhem.*

Shuyi Shao – Compilers for Predicting Communication in Parallel Networks, – *Co-Advised with Rami Melhem.*

Gayatri Mehta – Coarse-grained reconfigurable architectures for low-power – now a Tenure Track Professor at University of North Texas.

Ying Yu, Ph.D. A Content-Addressable Memory Assisted Intrusion Prevention Expert System for Gigabit Networks – now at Marvell Semiconductor.

Swapna R. Dontharaju, Ph.D. Design Automation for Low Power RFID Tags – now at Intel.

Shenchih Tung, Ph.D. An Architectural Approach for Reducing Power and Increasing Security of RFID Tags – Concurrent EDA, LLC.

Mustafa Baz – Ph.D. Optimization of Mapping onto a Flexible Low-power Electronic Fabric Architecture – now with Applied Decision Technologies, Inc. – *Co-Advised with Brady Hunsaker.*

Masters Theses Supervised

Ankita Sharma M.Sc. (professional) FPGA Emulation of NoC Simulation.

Liang Liao – M.Sc. Sensor networks for Green Buildings.

Haifeng Xu – M.Sc. Grid Computing for Sustainable Building Sensor Networks.

Yu Zhang – M.Sc. Simulation Of Multi-core Systems And Interconnections And Evaluation Of Fat-Mesh Networks.

Colin J. Ihrig, M.Sc. Static Timing Analysis Based Transformations of Super-Complex Instruction Set Hardware Functions – now a Ph.D. student.

Hariram Ravindran, M.Sc. (Professional).

Gerold Jospeh Dhanabalan, M.Sc. A Physical Implementation of a Reconfigurable Hardware Fabric with Low Power Extensions – now with Texas Instruments.

Justin Stander, M.Sc. Electronic Design Automation for an Energy-Efficient Coarse-Grain Reconfigurable Fabric Architecture – now with Concurrent, EDA, LLC.

Joshua M. Lucas, M.Sc. Technology Mapping for Circuit Optimization using Content-Addressable Memory – now with Lockheed Martin.

Joshua Fazekas, M.Sc. The VLIW-SuperCISC Compiler: Exploiting Parallelism from C Code Applications.

Salman Arif, M.Sc. (Professional) – now with Sun Microsystems.

Rajarshi Mukherjee, M.Sc. (with Prith Banerjee)

Current Student Supervision

Sebastien Ollivier – M.Sc. student (Fault-tolerance of emerging memories)

Chayanika Chaudhuri – Ph.D. student (Fault-tolerance of domain wall memories)

Nik Parshook – M.Sc. student (Thermal and Life-cycle Evaluation and Optimization from Tablets to Data centers)

Donald Kline – Ph.D. student (Networks on Chip, Compilers, Emerging Memories, Machine Learning

Seyedmohammad Seyedzadehdelcheh (Seyed) – Encoding Strategies for Mitigating Write Power in STT-MRAM – co-advised with Rami Melhem.

Colin Ihrig – Ph.D. student (Technology Dependent Delay Elements and Pipelining. Emulation of multi-core systems.)

Iheanyi Umez-Eronini – Ph.D. student (Control for Carbon Capture and Renewable Energy Integration) – co-advised with Zhi-Hong Mao.

Ian Moyer – M.S. student.

Ian Miller – M.S. student.

Hui Xu – Ph.D. student.

Shaobo Chen – M.S. student.

Hou Rui – M.S. student.

Dorene Dixon – M.S. student.

Xuebin Zhang – M.S. student.

Luo Hao – M.S. student.

Jiwei Shan – M.S. student.

Wahajuddin Syed – M.S. student.

Ross Dinsmore – M.S. student.

David Thompson – M.S. student.

Donald Kline Jr. B.Sc. student (NoC designs using emerging non-volatile memories).

Daniel Wright – B.Sc. student (Gait processing on Android devices).

Student Thesis Committees

University of Pittsburgh: Department of Electrical and Computer Engineering: (Ph.D) Socrates Demetriades, Mengjie Mao, Michael Moeng, Zhenyu Sun, Haifeng Xu, Yong Li, Yi-Chung Chen, Iheanyi Umez-Eroini, Xiuyi Zhou, Gayatri Mehta, Shenchih Tung, Swapna Dontharaju, Zhu Ding, Ying Yu, Baris Taskin, Rob Murawski, Joe Hines (M.Sc.): Yong Li, Liang Liao, Gerold Joseph Dhanabalan, Colin Ihrig, Justin Stander, Jeff Schuster, Johnny Ng, Josh Lucas, Joseph St. Onge, Josh Fazekas, Katrina Werger, Peter Hawrylak, Jake Repanshek, Josh Lucas, Dara Kusic, Kshitij Gupta (B.Sc.): Mark Klara, Marco Marsen, Ann Marie Grant, Nik Parshook, Kristin Roher, Alicia Beacom, Rebecca Vereb, Sara Wolfe

University of Pittsburgh: Department of Civil and Environmental Engineering: (Ph.D.) William Collinge

University of Pittsburgh: Department of Mechanical Engineering and Material Science: (Ph.D.) Justin DeBlois

University of Pittsburgh: Department of Industrial Engineering: (Ph.D.) Mustafa Baz

University of Pittsburgh: Department of Computer Science: (Ph.D.) Bryan Mills, Michael Moeng, Kiyeon Li, Socrates Demetriades, Ahmed Abousamra, Yuqiang Huang, Shuyi Shao, David Essary.

Virginia Tech: Department of Electrical and Computer Engineering: (Ph.D.) Nick Macias.

Northwestern University: Department of Electrical and Computer Engineering: (M.Sc.): Rajarshi Mukherjee

Professional Service

Editorial Service

Associate Editor, IEEE TSusC , IEEE Transactions on Sustainable Computing, 2016-*current.*

Associate Editor, TODAES , ACM Transactions on Design Automation of Electronic Systems, Guest Editor 2007, AE 2009-2012.

Associate Editor, special issue, TRETS: ACM Transactions on Reconfigurable Technology and Systems, special issue on Special Issue on Security in Reconfigurable Systems Design.

Associate Editor, special issue, PPL: Parallel Processing Letters, special issue on the Workshop for Large Scale Parallel Processing.

Associate Editor, JOLPE: Journal of Low Power Electronics, 2007 - *current.*

Associate Editor, IJCA: IASTED International Journal of Computers and Applications, 2004 - 2009.

Associate Editor, RPEE: Recent Patents in Electrical Engineering, 2007 - *current.*

Conference Committees

IGSC , Steering Committee (2018-current) General Chair (2019), Program Committee Chair (2018), International Green and Sustainable Computing Conference (IGSC), 2018.

Local Arrangements, ESWeek Local Arrangements Chair, ESWeek, 2016.

General Chair, GLSVLSI: General Chair, GLS Symposium on VLSI, 2015.

Program Committee Chair, GLSVLSI: Program Committee Chair, GLS Symposium on VLSI, 2013, 2014.

Program Committe, IGCC/IGSC: International Green (and Sustainable) Computing Conference, 2014-*current*

Program Committee, DAC: Program Committee, The Design Automation Conference, 2011 - *current*.

Program Committee, PACT: Program Committee, The Conference on Parallel Architectures and Compilation Techniques, 2011, 2014.

Program Committee, ISSS-CODES Program Committee, 2011-2013.

Organizing Committee, WD_2AT: Organizing Committee, Workshop on Diversity in Design Automation and Test, 2011]

General Chair, INTERACT: General Chair, Steering Committee Chair, Workshop on the interaction of compilers and computer architecture, 2009-2011.

University Booth, DAC: University Booth Coordinator, Design Automation Conference, 2005 - 2006. SIGDA Advisor, 2006 - 2009.

General Chair, MSE: Microelectronic Systems Education Conference, 2011.

Program Committee, DAC Ph.D. Forum Program Committee, Chair, DAC Ph.D. Forum, 2008 - *current*.

Steering Committee, WLSPP Steering Committee, Workshop on Large-Scale Parallel Processing at the International Parallel & Distributed Processing Symposium, 2008 - *current*. *Publicity chair*, 2008.

Organizing Committee, Special Session in MPP at ADPCM/IPDPS: Organizing Committee, Special Session in Massively Parallel Processing at the Workshop on Advances in Parallel and Distributed Computing Models (ADPCM) at the International Parallel & Distributed Processing Symposium, 2007.

Program Committee, MSE: Program Committee, Microelectronic System Education Conference, 2005 - *current*.

Program Committee, WMPP: Program Committee, Workshop on Massively Parallel Processing, 2005.

Technical Committee, ICPP: Technical Committee, International Conference on Parallel Processing, 2005 - *current*.

Technical Committee, PDCS: Technical Committee, IASTED Parallel and Distributed Computing and Systems Conference, 2003-2005, 2007 - *current*.

Professional Society Memberships

Senior Member, IEEE/IEEE Computer Society

Senior Member, Association for Computing Machinery (ACM)

Special Interest Group in Design Automation (SIGDA) – **Executive Committee Member, roles, Technical activities chair, Finance chair, Vice-Chair**