The Manufacturing Process

For a great tour through the IC manufacturing process and its different steps, check

http://www.fullman.com/semiconductors/semiconductors.html
CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process
Typical operations in a single photolithographic cycle (from [Fullman]).

- Oxidation
- Photoresist coating
- Stepper exposure
- Photoresist development
- Acid etch
- Spin, rinse, dry
- Process step
- Photoresist removal (ashing)
CMOS Process at a Glance

1. Define active areas
   Etch and fill trenches

2. Implant well regions

3. Deposit and pattern polysilicon layer

4. Implant source and drain regions and substrate contacts

5. Create contact and via windows
   Deposit and pattern metal layers
Patterning of SiO₂

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

(d) After development and etching of resist, chemical or plasma etch of SiO₂

(e) After etching

(f) Final result after removal of resist
**N Well Process**

![Diagram showing N Well Process](image)

**FIG 1.33** Inverter cross-section

- **SiO**
- **n+ diffusion**
- **p+ diffusion**
- **polysilicon**
- **metal1**
Well and Substrate Taps

- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line

![Diagram of inverter mask set with labels for GND, VDD, substrate tap, nMOS transistor, pMOS transistor, and well tap.](image-url)
Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
FIG 1.36 Cross-sections while manufacturing the n-well
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO₂ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO₂
Oxidation

- Grow SiO$_2$ on top of Si wafer
  - 900 – 1200 C with H$_2$O or O$_2$ in oxidation furnace
Spin on photoresist
- Photoresist is a light-sensitive organic polymer
- Softens where exposed to light
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!
- Only attacks oxide where resist has been exposed
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step

\[ \text{SiO}_2 \]

p substrate
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO₂, only enter exposed Si
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps
Self Aligned Gate:

Poly masks the channel
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor
Polysilicon Patterning

- Use same lithography process to pattern polysilicon
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion
N-diffusion cont.

- Strip off oxide to complete patterning step
**Figure 1.38** Cross-sections while manufacturing p-diffusion, contacts, and metal

- **P substrate contact**
- **N well contact**

(a) p-substrate

(b) p-substrate

(c) p-substrate

Thick field oxide

Metal

Thick field oxide
Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact.
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

Diagram:
- p substrate
- Thick field oxide
- n well
- n+
- p+
Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

Diagram:
- Metal
- Thick field oxide
- p substrate
- n well
CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO$_2$ insulator, etching of via’s, deposition and patternning of second layer of Al.
Advanced Metallization
Advanced Metallization

Dual damascene IC process

- Oxide deposition
- Stud lithography and reactive ion etch
- Wire lithography and reactive ion etch
- Stud and wire metal deposition
- Metal chemical-mechanical polish

Source: IBM Corp.
Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size $f =$ distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3 \ \mu m$ in 0.6 $\mu m$ process
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)
- Rules from
  - Manufacturing process (antenna rules)
  - Final result (shorts/opens)
- Could be
  - Electrical – maximum current
  - Mechanical – surface planarity
  - Thermal - overheating
  - Optical – mask requirements
  - Characterization – only some size transistors well characterized
- Rules used to be 3 pages, now a book, soon worse…
Simplified Design Rules

- Conservative rules to get you started

Diagram showing spacing and width rules for Metal1 and Metal2, along with diffusion and polysilicon layers.
Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is \(4\lambda / 2\lambda\), sometimes called 1 unit
  - In \(f = 0.6 \, \mu m\) process, this is 1.2 \(\mu m\) wide, 0.6 \(\mu m\) long
# CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td><img src="image" alt="Yellow" /></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td><img src="image" alt="Green" /></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td><img src="image" alt="Green" /></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td><img src="image" alt="Red" /></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td><img src="image" alt="Blue" /></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td><img src="image" alt="Magenta" /></td>
</tr>
<tr>
<td>Contact To Poly</td>
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<td><img src="image" alt="Black" /></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td><img src="image" alt="Black" /></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td><img src="image" alt="Black" /></td>
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</tbody>
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### Layers in 0.25 μm CMOS process

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1, m2, m3, m4, m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct, v12, v23, v34, v45, nwc, pwc</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif, pdif, nfct, pfct</td>
</tr>
<tr>
<td>select</td>
<td>nplus, pplus, prb</td>
</tr>
</tbody>
</table>
Intra-Layer Design Rules

Minimum size, spacing rules
Transistor Layout (inter layer rules)
Vias and Contacts

Via

Metal to Poly Contact

Metal to Active Contact

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Manufacturing
Select Layer

substrate contact

well contact

Substrate

Well

Select
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A’
Layout Editor (what is missing?)
Design Rule Checker

poly_not_fet to all_diff minimum spacing = 0.14 um.
Sticks Diagram

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Stick diagram of inverter
Gate Layout

- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - $V_{DD}$ and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts
Example: Inverter

(a) 

(b) 

Well Tap

Substrate T
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 \( V_{DD} \) rail at top
- Metal1 GND rail at bottom
- 32 \( \lambda \) by 40 \( \lambda \)
Stick Diagrams

- **Stick diagrams** help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers
Wiring Tracks

- A *wiring track* is the space required for a wire
  - $4\lambda$ width, $4\lambda$ spacing from neighbor $= 8\lambda$ pitch
- Transistors also consume one wiring track
Well spacing

- Wells must surround transistors by 6 $\lambda$
  - Implies 12 $\lambda$ between opposite transistor flavors
  - Leaves room for one wire track
Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in $\lambda$
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

\[ Y = (A + B + C) \overline{D} \]
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

\[ Y = (A + B + C) \square D \]
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

\[ Y = (A + B + C) \square D \]